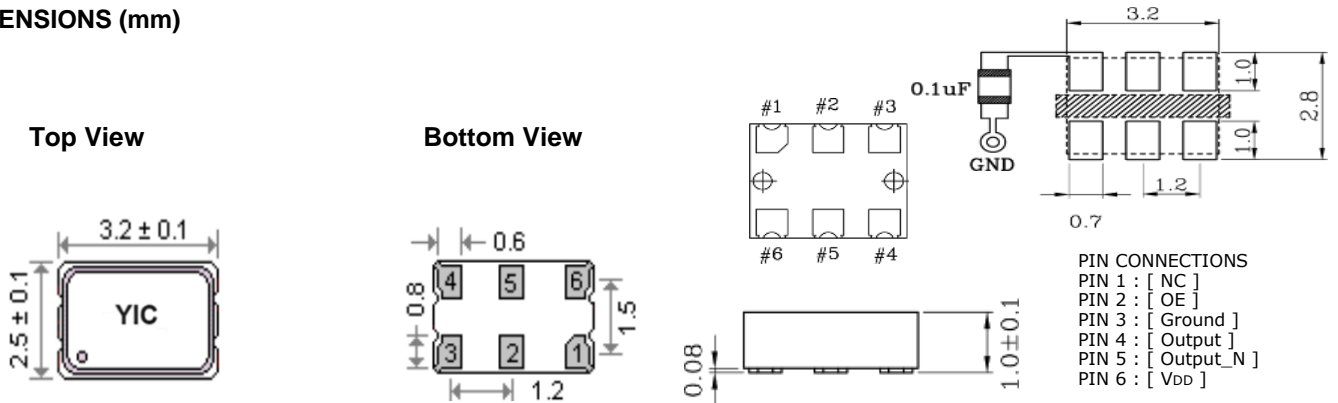


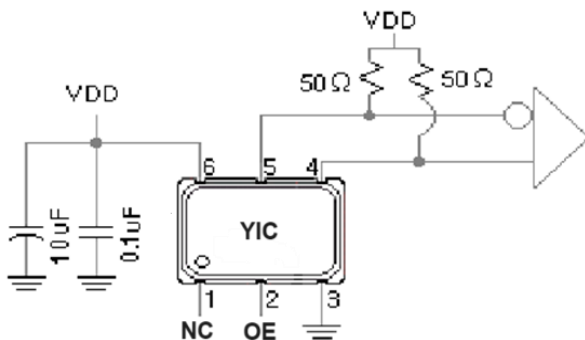
● SPECIFICATION

| | | | |
|--------------------------------|--|--------------------|--------------------|
| Model | OC -S3 Series | | |
| Power supply voltage | 1.8V DC $\pm 5\%$ | 2.5V DC $\pm 10\%$ | 3.3V DC $\pm 10\%$ |
| Output level | CML | | |
| Frequency range | 15.000 MHz ~ 2100.00 MHz | | |
| Storage temperature range | - 55°C ~ + 125°C | | |
| Operation temperature range | - 20°C ~ + 70°C , - 40°C ~ + 85°C , - 40°C ~ + 125°C , specify | | |
| Frequency stability | ± 25 ppm ~ ± 100 ppm | | |
| Current consumption | 90 mA (max) (3.3V) , 80 mA (max) (2.5V) , 70 mA (max) (1.8V) | | |
| Output Load | 50 Ω to VDD | | |
| Output voltage level (VOH) | VDD - 0.085V (min) , VDD = (max) | | |
| Output voltage level (VOL) | VDD - 0.6V (min) , VDD - 0.32V (max) | | |
| Differential Output voltage | 200 mV (min) , 600m V (max) | | |
| Start-up Time | 8 m sec (max) | | |
| Duty cycle | 45% ~ 55% | | |
| Enable input voltage (VIH) | 0.7 x VDD (min) | | |
| Disable input voltage (VIH) | 0.3 x VDD (max) | | |
| RISE / FALL TIME (20% / 80%) | 0.35 nS (max) | | |
| Phase Jitter RMS (12KHz~20KHz) | 150 fS (min) , 300 fS (max) | | |
| Aging at Ta = +25°C | ± 3 ppm (max) @ first year | | |

● DIMENSIONS (mm)



● CML Test Circuit



● OUTPUT WAVEFORM

